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Complete if Known Substitute for form 1449A/PTO Application Number 09/741,821 INFORMATION DISCLOSURE December 22, 2000 Filing Date STATEMENT BY APPLICANT First Named Inventor Terry R. Lee Art Unit 2181 (use as many sheets as necessary) Examiner Name Not Yet Assigned M4065.0406/P406 of 1 Attorney Docket Number Sheet 1

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	U.S. PATENT DOCUMENTS							
Examiner Initials*	Cite No.1	Document Number Number-Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Technology Center 2 0 Passages or Relevant Figures Appear			
(W)	Α	4,974,152	11/27/1990	Guiffant et al.				

	FOREIGN PATENT DOCUMENTS							
Examiner Initials*	Cite No.1	Foreign Patent Document	Publication Date	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear			
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)	MM-DD-YYYY			T ⁶		
wn	Α	WO 99/30240	06/17/1999					
W /		(PCT/US98/25181)						
W	В	WO 99/19874	04/22/1999					
. 7		(PCT/US98/21449)						

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m	Α	YASUHIRO KONISHI et al., "Interface Technologies for Memories and ASICs – Review and Future Direction – ", IEICE Transactions on Electronics, Vol. E82-C. No. 3 March 1999.			
W	В	ALFREDO MONCAYO et al., "Physical Layer Design of a 1.6 GB/s DRAM Bus", 1999 IEEE.			

^{*}EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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